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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,710	08/16/2001	Lloyd E. Thorsbakken	RA 5372 (33012/317/101)	3426

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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,710	THORSBAKKEN ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 6/9/05. Currently claims 1-20 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. *Claims 1-5 and 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell in view of Downey (US 5881294 A) and Lentz (US 6047348 A).*

Regarding claim 1, Bell discloses the first and second data buses (e.g., col. 5, lines 7-9) and a circuit responsively coupled to both which combines the buses into a logical bus having a third set of different characteristics (e.g., col. 5, lines 16-19), and the selector for multiplexing (e.g., col. 17, lines 58-63). While Bell discloses an integral multiplexed mode of operation (e.g., col. 5, lines 7-9, "64-bit mode") he neglects to mention particular details of that operating mode; however, these details are disclosed by Downey. Downey discloses a single set of interrupt handling logic coupled to the multiple sources (e.g., Fig. 6, col. 11, lines 38-45). It would have been obvious to one of ordinary skill in the art to combine Downey with Bell, because Downey shows a means to respond to interrupts from multiple locations using a convenient centralized handling logic. Bell does not expressly mention the particular selector details;

however, this detail is disclosed by Lentz, who teaches a selector connecting the first bus to the third and second interfaces (e.g., Figure 2, "215", "217"), and the second bus to the first and second interfaces (e.g., Figure 4). It would have been obvious to combine Lentz with Bell because Lentz shows the express details of a system where two interfaces are connected to form a logical bus as taught in Bell.

Regarding claim 2, Bell also discloses the characteristics are maximum transfer rates and that the third rate is greater than either of the first two (e.g., col. 5, lines 16-19).

Regarding claim 3, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 4, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Regarding claim 5, Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9).

Regarding claim 11, Bell discloses first and second data bus provision (e.g., col. 5, lines 7-9) and combining the buses into a logical bus with third set of characteristics (e.g., col. 5, lines 16-19). While Bell discloses an integral multiplexed mode of operation (e.g., col. 5, lines 7-9, "64-bit mode") he neglects to mention particular details of that operating mode; however, these details are disclosed by Downey. Downey discloses a single set of interrupt handling logic coupled to the multiple sources to produce a bus (e.g., Fig. 6, col. 11, lines 38-45). It would have been obvious to one of ordinary skill in the art to combine Downey with Bell, because Downey shows a means to respond to interrupts from multiple locations using a convenient centralized handling

logic. Bell does not expressly mention the particular selector details; however, this detail is disclosed by Lentz, who teaches a selector connecting the first bus to the third and second interfaces (e.g., Figure 2, "215", "217"), and the second bus to the first and second interfaces (e.g., Figure 4). It would have been obvious to combine Lentz with Bell because Lentz shows the express details of a system where two interfaces are connected to form a logical bus as taught in Bell.

Regarding claim 12, Bell also discloses first and second data transfer rates as the characteristics and a third transfer rate characteristic greater than either of the said first and second (e.g., col. 5, lines 16-19).

Regarding claim 13, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 14, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Regarding claim 15, Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9).

Regarding claim 16, Bell discloses first and second means for performing data processing functions (e.g., col. 5, lines 20-25, "processor 10 or other processors", "90A and 90B"), first and second means coupled between processing means for transferring data (e.g., col. 5, lines 7-9) and means for combining the buses into a logical transferring means with third set of characteristics (e.g., col. 5, lines 16-19), and the selector for multiplexing (e.g., col. 17, lines 58-63). While Bell discloses an integral multiplexed mode of operation (e.g., col. 5, lines 7-9, "64-bit mode") he neglects to mention particular details of that operating mode; however, these details are disclosed

by Downey. Downey discloses a single set of interrupt handling logic coupled to the multiple sources (e.g., Fig. 6, col. 11, lines 38-45). It would have been obvious to one of ordinary skill in the art to combine Downey with Bell, because Downey shows a means to respond to interrupts from multiple locations using a convenient centralized handling logic. Bell does not expressly mention the particular transferring means; however, this detail is disclosed by Lentz, who teaches alternating transfers from the first and second transferring means to provide logical transferring means having a third set of characteristics (e.g., Figure 2, "215", "217"; col. 4, line 64—col. 5, line 1). It would have been obvious to combine Lentz with Bell because Lentz shows the express details of a system where two interfaces are connected to form a logical bus as taught in Bell.

Regarding claim 17, Bell also discloses first and second data transfer rates as the characteristics and a third transfer rate characteristic greater than either of the said first and second (e.g., col. 5, lines 16-19).

Regarding claim 18, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 19, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Regarding claim 20, Bell also discloses the rate is 33 MHz (e.g., col. 5, line 9).

2. *Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (US 6330630 B) in view of Lentz (US 6047348 A).*

Regarding claim 6, Bell discloses buses coupled between components (e.g., col. 5, lines 7-9) and a circuit responsively coupled to both, which combines the buses into a logical bus (e.g., col. 5, lines 16-19), and the selector for multiplexing (e.g., col. 17, lines 58-63). Bell does not expressly mention the particular selector details; however, this detail is disclosed by Lentz, who teaches a selector connecting the first bus to the third and second interfaces (e.g., Figure 2, "215", "217"), and the second bus to the first and second interfaces (e.g., Figure 4). It would have been obvious to combine Lentz with Bell because Lentz shows the express details of a system where two interfaces are connected to form a logical bus as taught in Bell.

Regarding claim 7, Bell also discloses the first and second characteristics of the buses and the third different characteristic (e.g., col. 5, lines 16-19).

Regarding claim 8, Bell also discloses first and second data transfer rates as the characteristics and a third transfer rate characteristic greater than either of the said first and second (e.g., col. 5, lines 16-19).

Regarding claim 9, Bell also discloses the third transfer rate is the sum of the first and second rates (e.g., col. 17, lines 60-63).

Regarding claim 10, Bell also discloses the first and second maximum transfer rates are equal (e.g., col. 5, lines 7-9).

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection. Certain arguments communicated 6/9/05 are

considered pertinent to the new rejection; however, the response below reflects new grounds of rejection necessitated by amendment,

Applicant argues that the "'switching' limitation distinguishes over Bell in that any suggestion in Bell to 'combine' the two busses is without disclosure" (p. 11); the Examiner concurs and has provided a reference that teaches the switching details of the combination disclosed by Bell, said reference (Lentz) used in combination with Bell.

Applicant further argues that no motivation has been provided for the combination of Downey with Bell; however, this can be further clarified. Bell discloses the teaching of combining two buses but neglects to mention the details of combining the interrupts thereon. One of ordinary skill in the art would be motivated to seek this particular solution in the arts, and it would have been obvious to use the handling of interrupts from multiple sources as taught in Downey as a solution to the problem presented by Bell by combining buses without an express solution as to how to combine the interrupts.

Applicant further argues that although "arguably Downey routes interrupts through a common circuit, that circuit does not have any data bus selection capability" and there is a "need to handle both data and control signals over the claimed busses" that exclude the simple application of Downey to Bell (p. 13); however a nexus between the interrupt handler and data handling capability does not find support in the claims. Bell discloses the combination of buses but omits certain features required in its implementation; regarding data handling capability, the express details of that feature

are provided by Lentz; regarding common interrupt capability, the express details of that feature are provided by Downey.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Simmons (US 5936953 A) shows particular switching details of bus combination (e.g., Figure 6).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

REHANA PERVEEN
PRIMARY EXAMINER
8/8/05